Securing interruptible enclaved execution on small microprocessors

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Joint work with:
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Programmers (unknowingly) use them for security!

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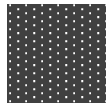

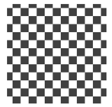

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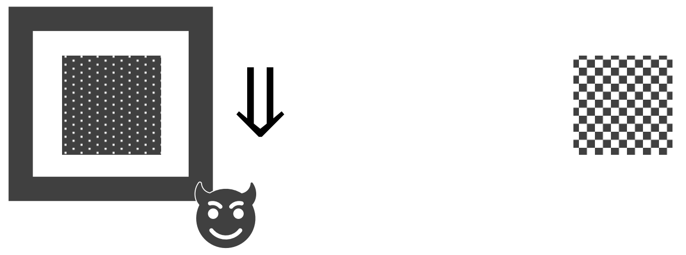

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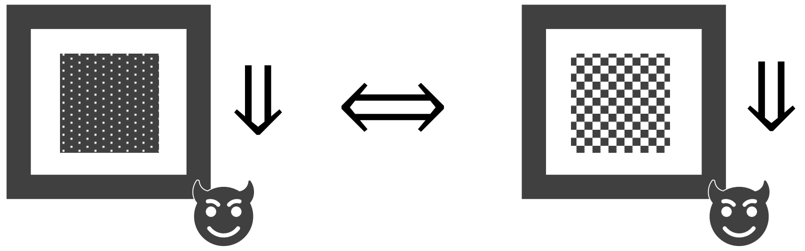

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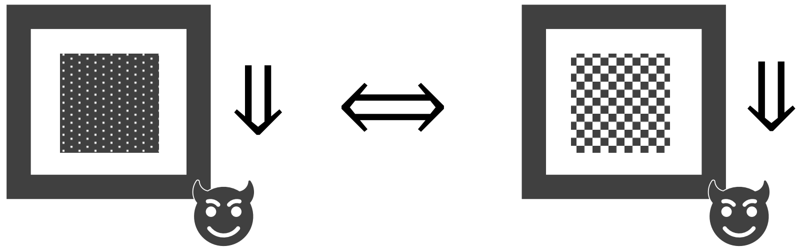

Isolation **security** ≜ equiconvergence under any attacker, i.e., **contextual equivalence**

Goals

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(**H**) High-language ≈

ISA with an isolation mechanism ≈
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We want:

- isolation of **L** **not weaker** than that of **H**, and
- backwards compatibility

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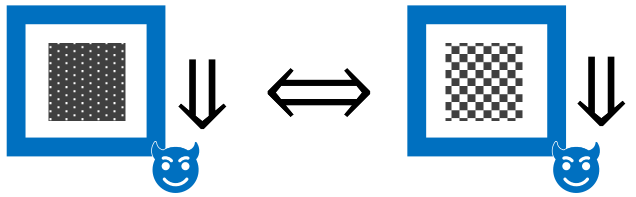

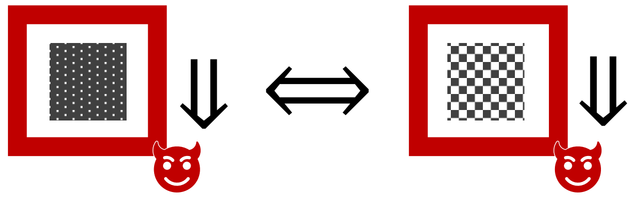

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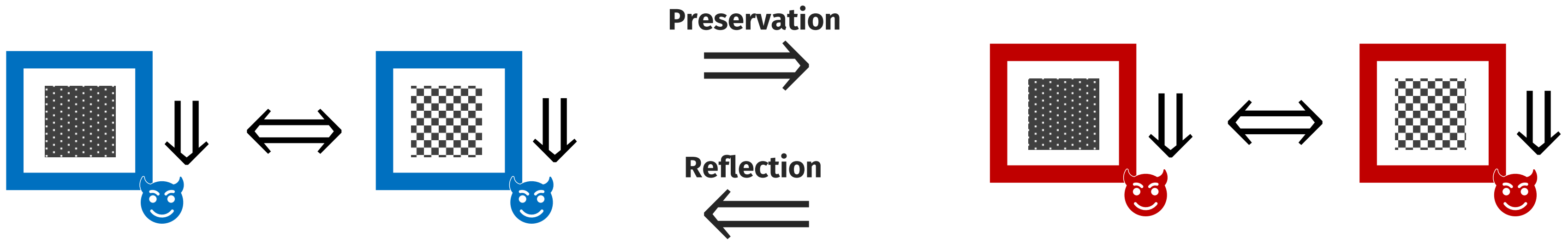

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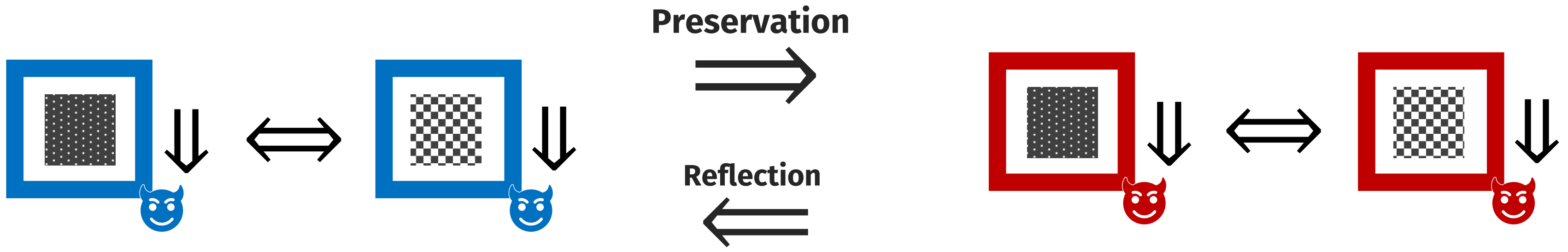

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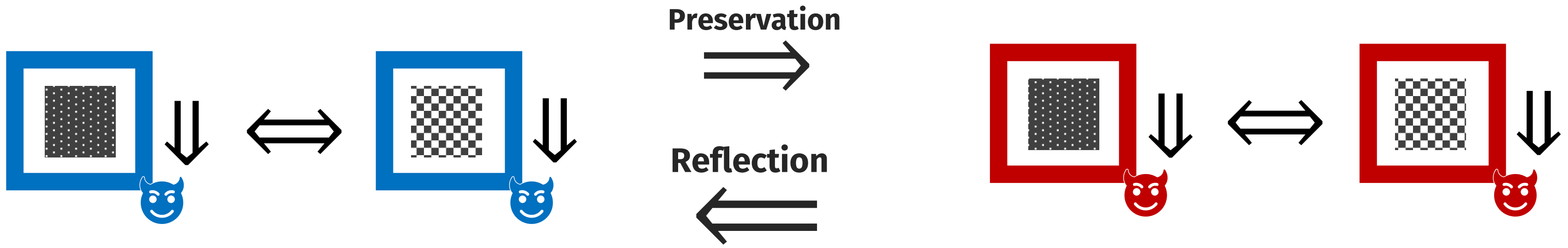

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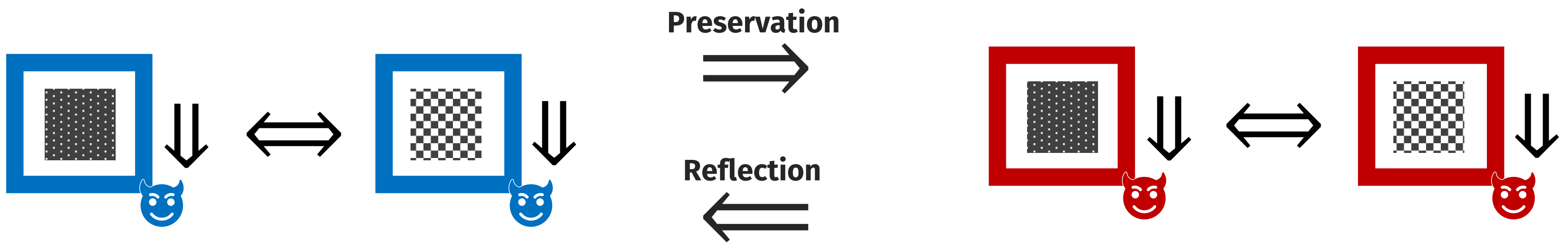

i.e., **H** and **L** are fully abstract

Our case: enclaves as isolation mechanism

"Dedicated" execution environments for secure remote computation

- **Attacker model:** everything outside the enclave (incl. OS, I/O devices, ...)
- Code and data integrity and confidentiality, via attestation & access control

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Sancus

Enclaved-execution (embedded) architecture on top of TI MSP430

- RISC instruction set
- Each instruction may take a different amount of time
- 64KB of memory, split into **protected** (enclaved) and **unprotected**
- No speculative execution, no interruptible enclaves, …

https://distrinet.cs.kuleuven.be/software/sancus/

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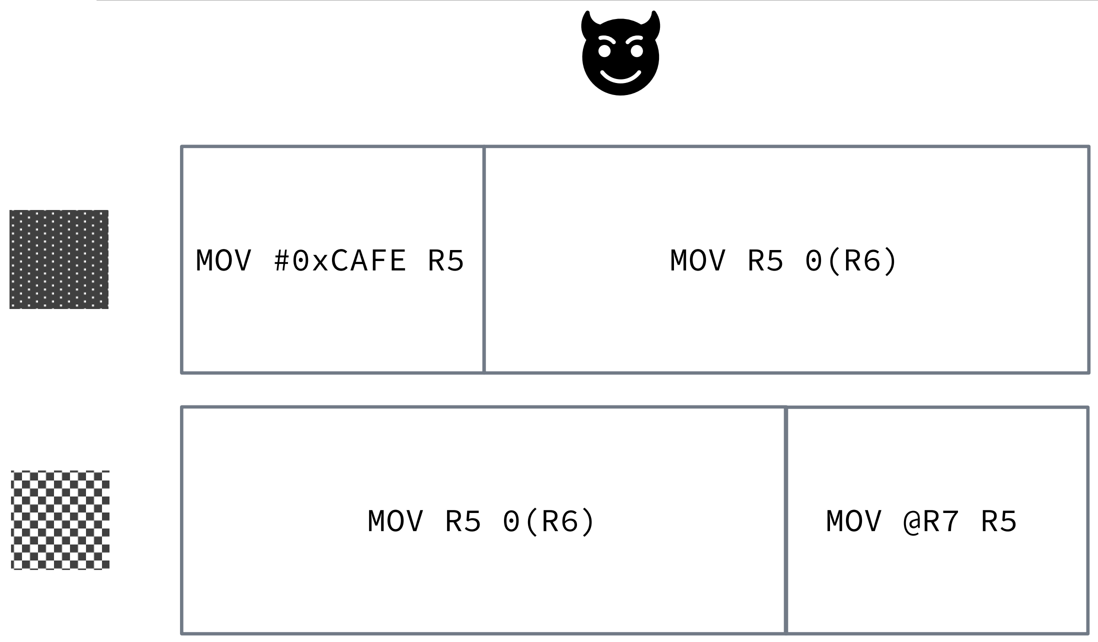

```
MOV #0xCAFE R5    MOV R5 0(R6)
MOV R5 0(R6)      MOV @R7 R5
```

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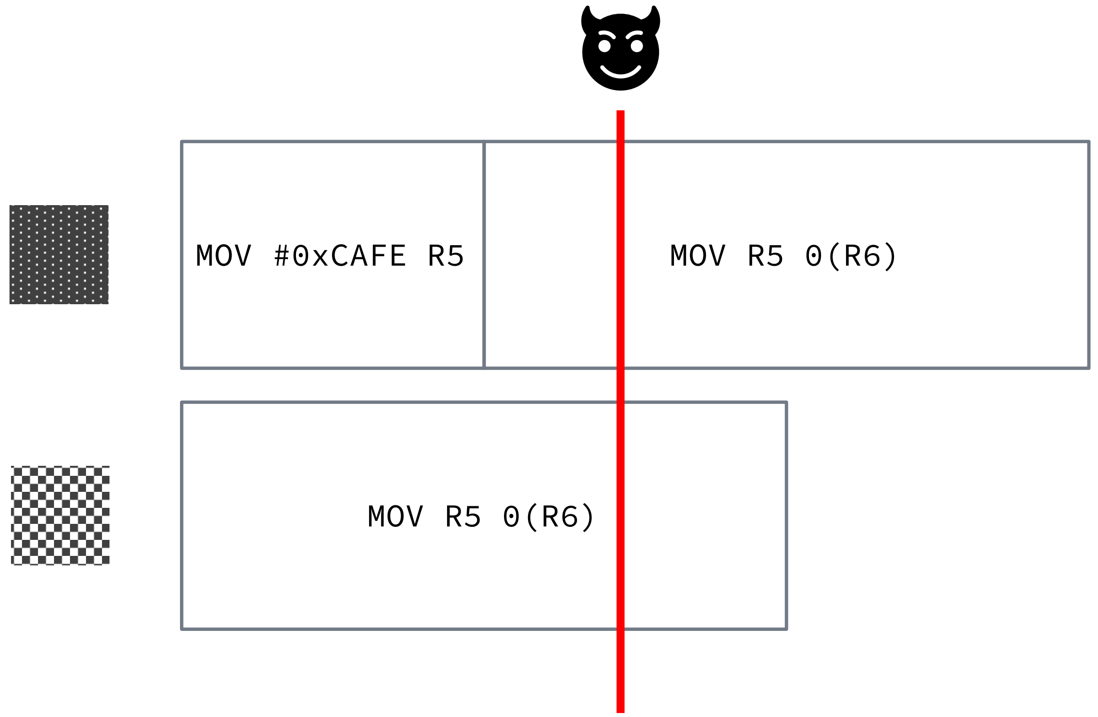

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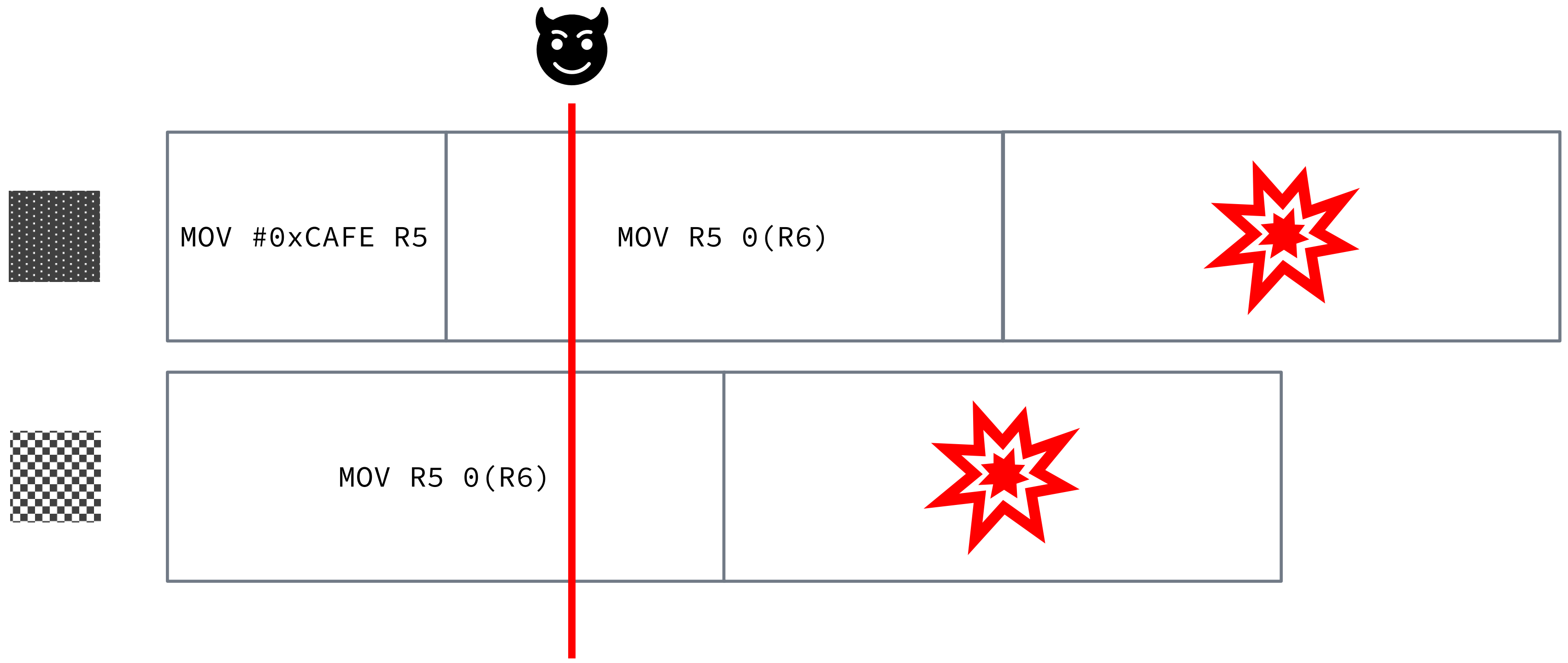

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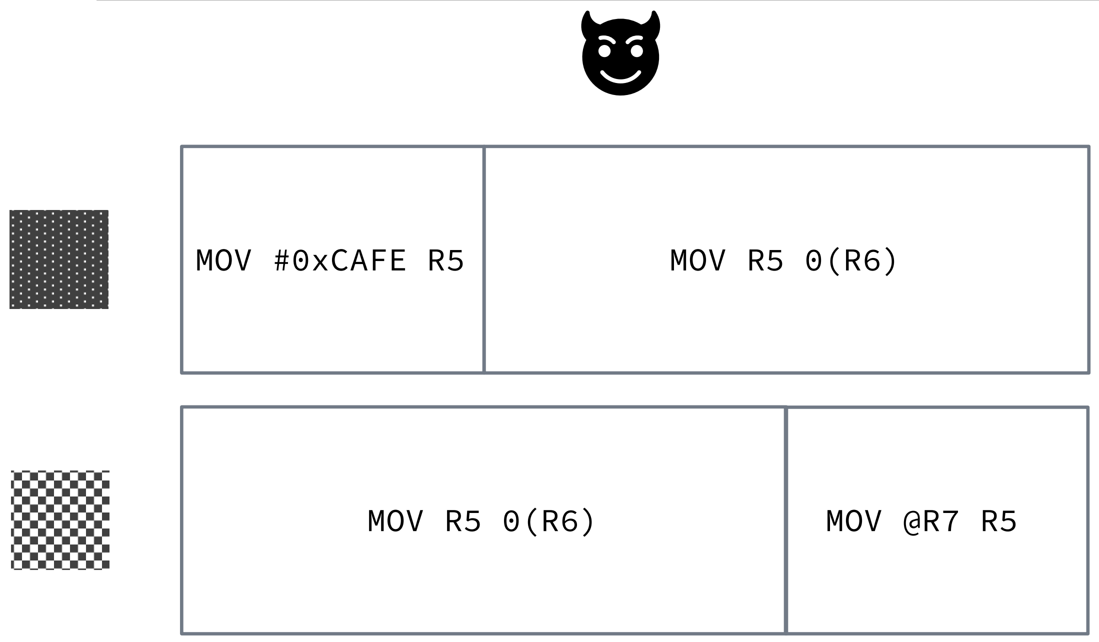

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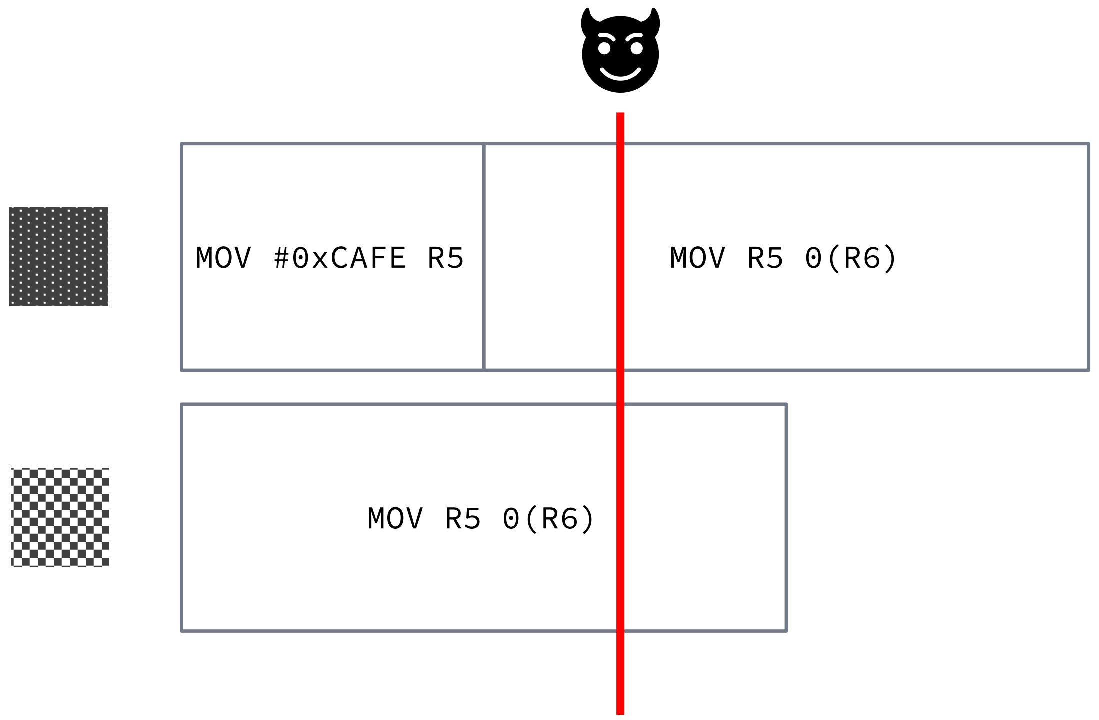

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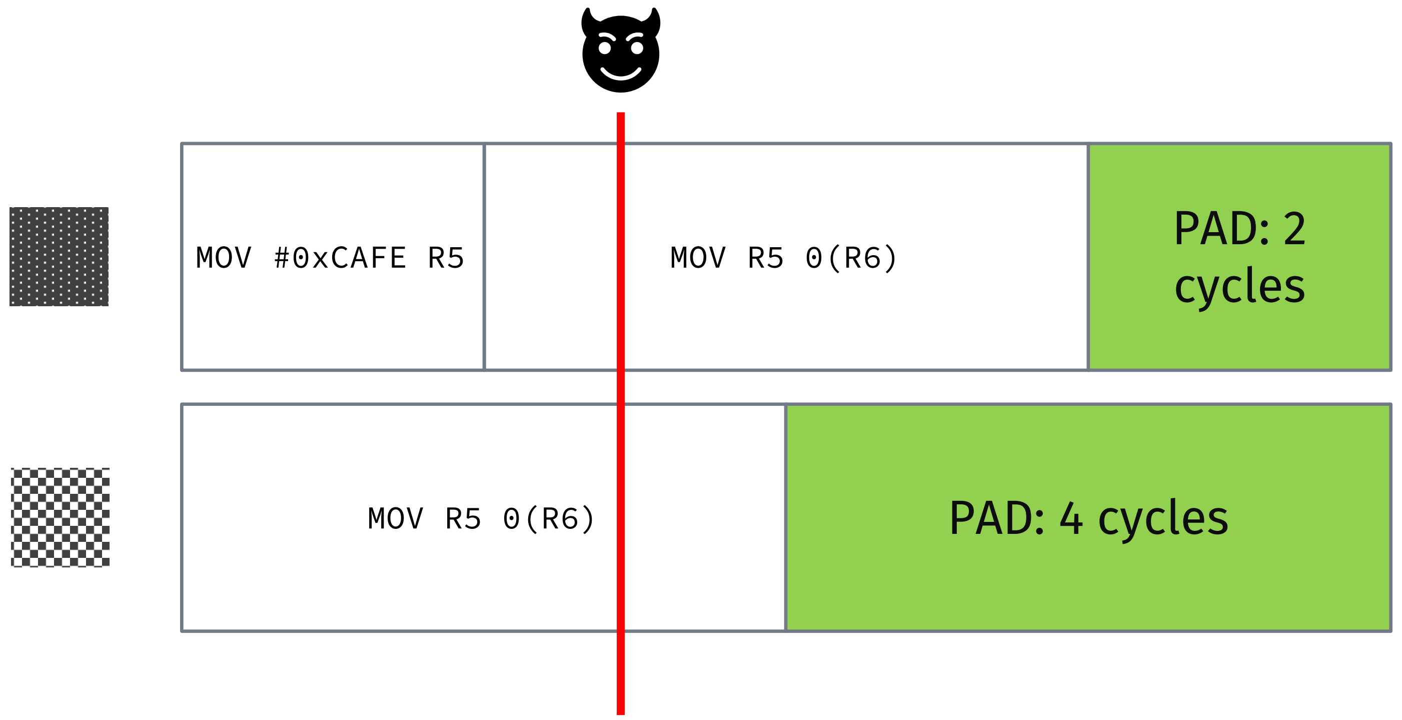

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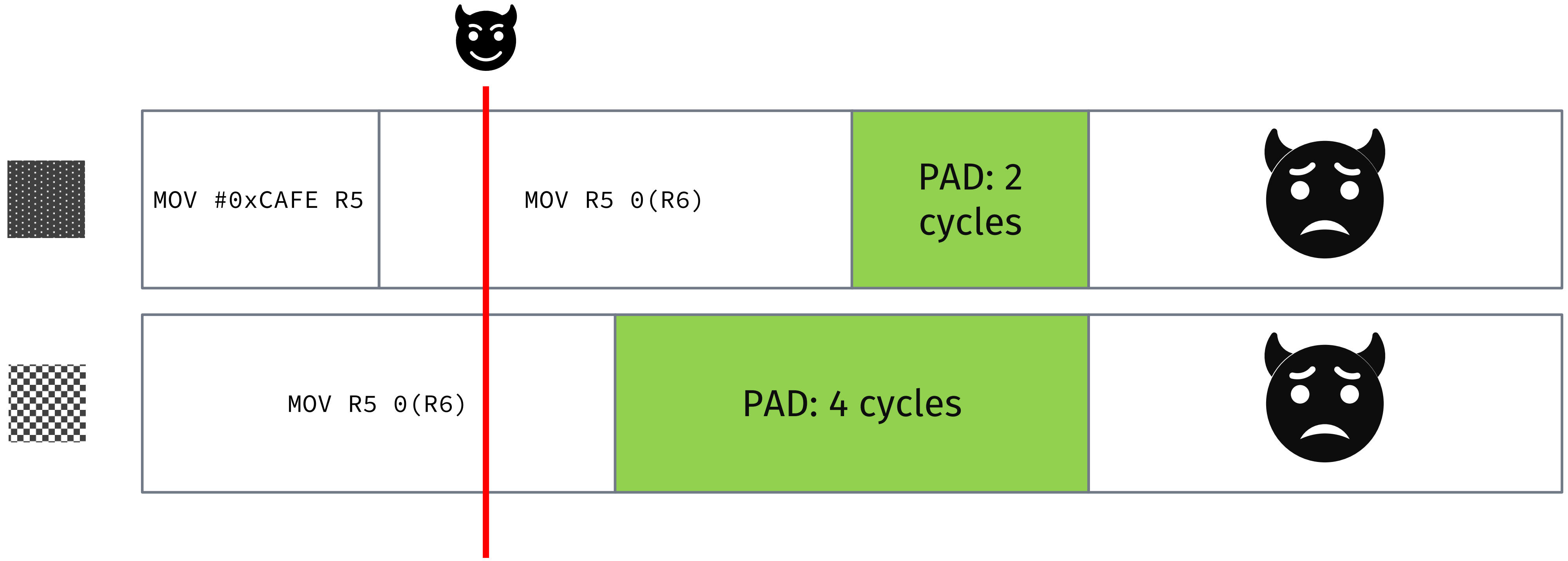

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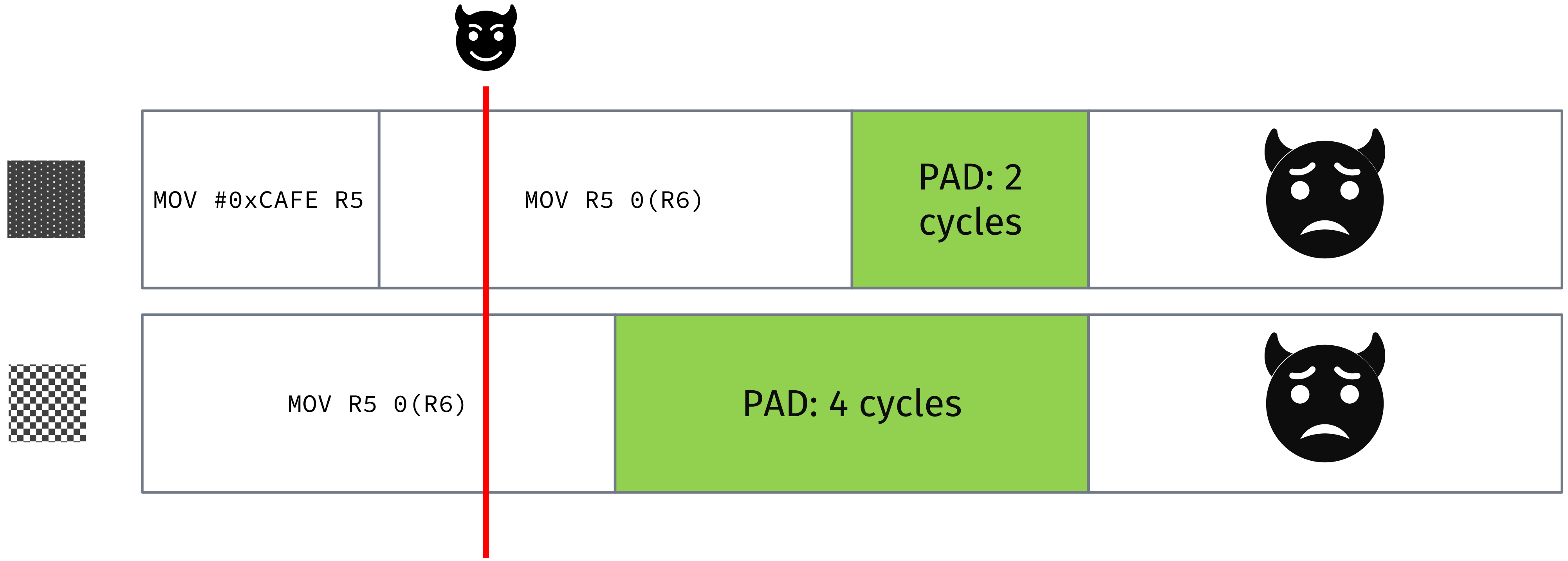

Is Nemesis fixed?

Nope, it is not!

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- … And a few other subtle cases!

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How do we know we are done? 😰

1. Model Sancus as **H** and **L**
2. Prove **full abstraction**, i.e., preservation + reflection!

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High-language is Sancus^H

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Interrupts handled in constant-time inside enclaves

Attackers:

- **memory outside enclave**, including ISR
- **I/O device** for raising interrupts/counting cycles/…

Step 2: full abstraction, reflection

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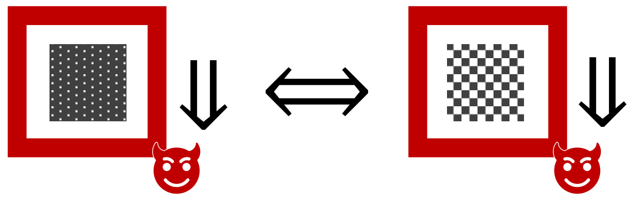

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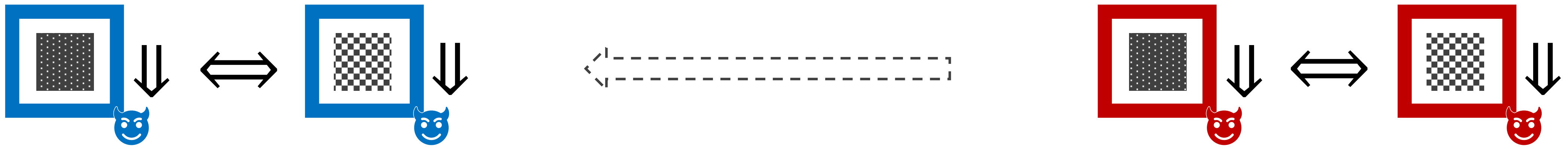

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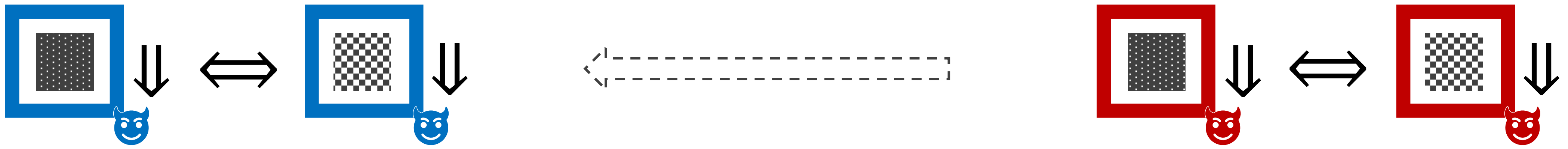

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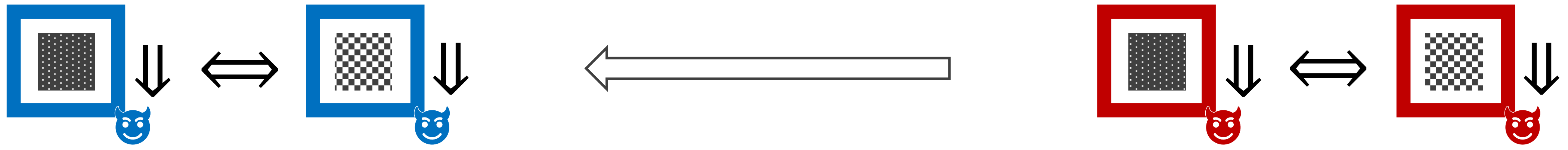

- This is the easy part!
- Attackers in Sancus^{H} ⊆ Attackers in Sancus^{L}

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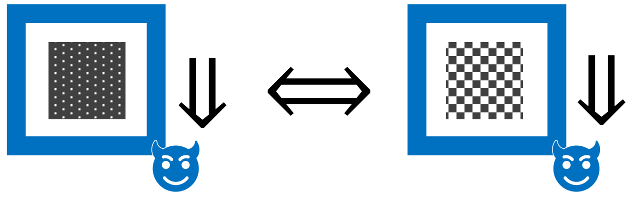

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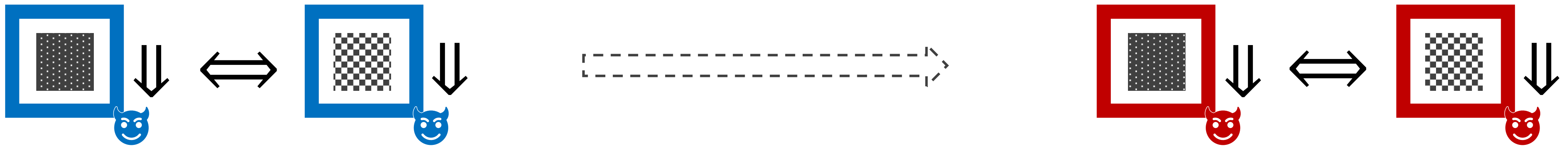

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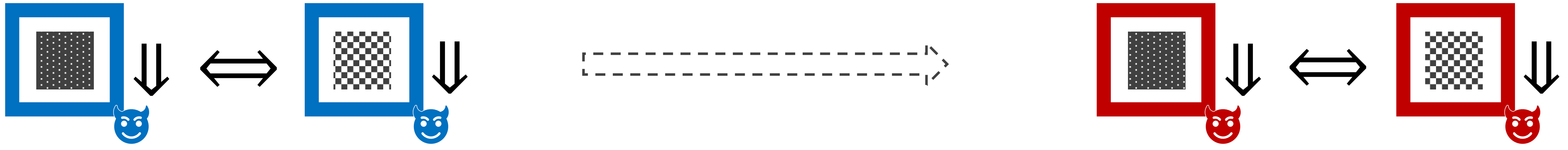
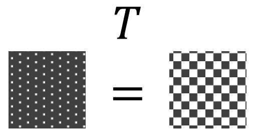
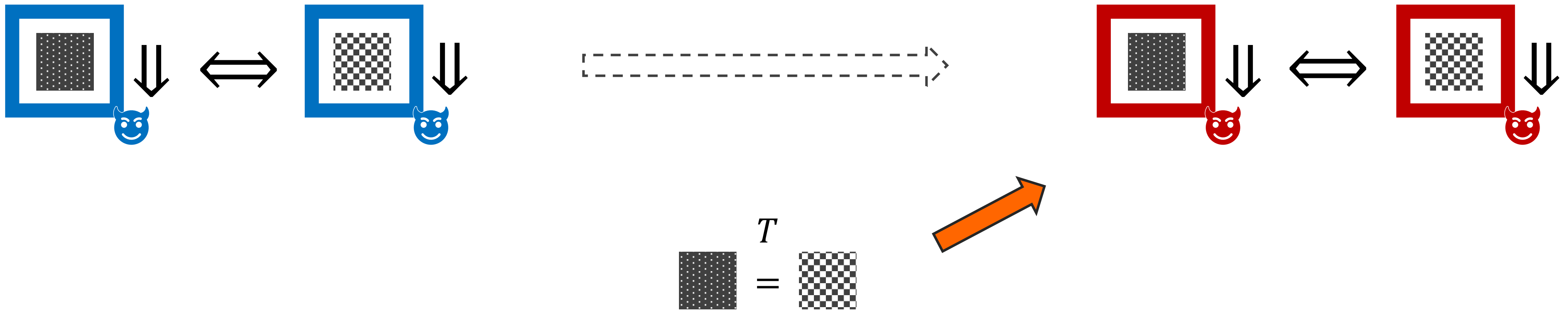




Notion of observable behavior in Sancus^{L}:
traces and trace equivalence

Step 2: full abstraction, preservation



- Trace equivalence ⇒ no Sancus^L attacker distinguishes the two programs
- This amounts to show that our **mitigations are enough**!

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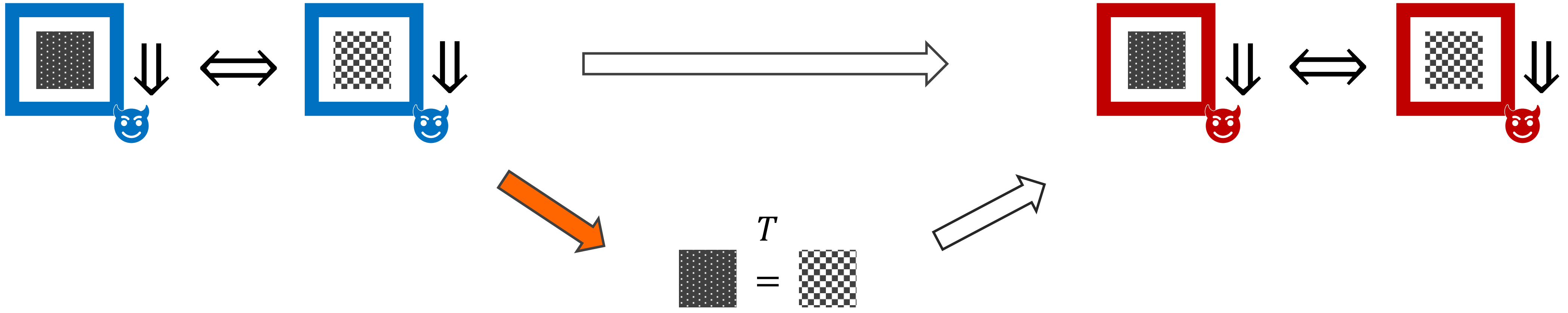

$\Downarrow$ $\Longleftrightarrow$ $\Downarrow$
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$\overset{T}{=}$

- Contrapositive: ▩ $\overset{T}{\neq}$ ▨ implies $\exists$ ☐ . ▩ $\Downarrow$ $\wedge$ ▨ $\Uparrow$ (+ symm)
- Proof by **backtranslation**:
  - Given a witness of non-trace equality, we build a witness of a source attack
  - Source attackers have fixed memory, traces are not limited:
    - Attacker strategy encoded in the I/O device!

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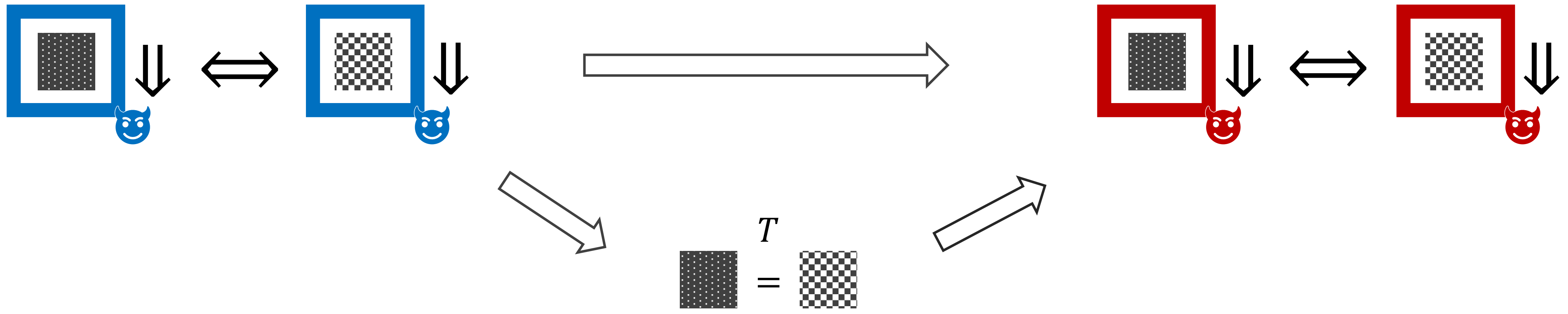
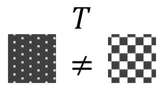
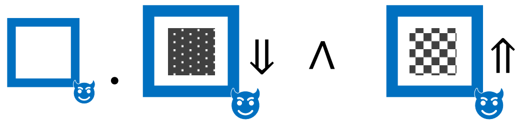


- Contrapositive:  implies ∃  (+ symm)
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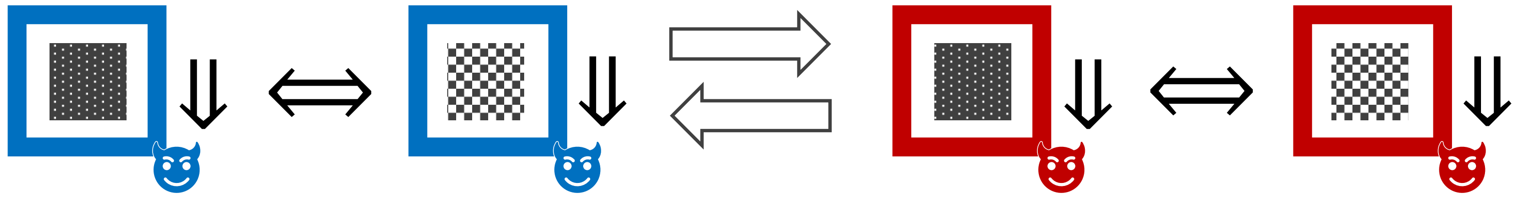
Full abstraction gives you more... 🙃

For free: preservation of robust ⇓-sensitive/⏱-sensitive non-interference:
- Standard, well-studied notion in secure compilation
- Easy **Corollary** of full abstraction!

Other notions of robust non-interference preservation:
- **⇓-insensitive/⏱-sensitive**: corollary of full abstraction + HP of equiconv. in Sancus^{H}
- **stepwise ⇓-sensitive/⏱-sensitive**: for free as corollary of FA!
- **⏱-insensitive:** not meaningful (we know our attacker measures time!)

Conclusions

- **Initial question:** is there a way to add processor features securely while keeping backwards-compatibility?
- **Proposal:** use full abstraction, well-fitted for the scope
- **Our case:** proved that Sancus^H and Sancus^L are fully abstract



Future work

- What about **other features** (e.g., caches, spec. execution, …)?
- Can we make the full abstraction approach **compositional**?
- Can we deal with stronger attackers?
- Also, what about **quantitative** measures of security?

Thanks

Questions?